Year	Title of paper	Co-authors	Affiliation
2019	A Power-efficient, Bi-directional Readout Interface Circuit for Cyclic-voltammetry Electrochemical Sensors	Yi-Chia Chen, Shao-Yung Lu, Jui-Hsiang Tsai and Yu-Te Liao	National Chiao Tung University
	Primitive Concept Identification In A Given Set of Wafer Maps	Ahmed Wahba[1], Chuanhe Shan[1], Li-C. Wang[1] and Nik Sumikawa[2]	[1]UCSB [2]NXP
2018	A 1.86mJ/Gb/Query Bit-Plane Payload Machine Learning Processor in 90nm CMOS	Fang-Ju Ku, Tung-Yu Wu, Yen-Chin Liao, Hsie-Chia Chang, Wing Hung Wong and Chen-Yi Lee	National Chiao Tung University
	Using Range-equivalent Circuits for Facilitating Bounded Sequential Equivalence Checking	Yung-Chih Chen, Wei-An Ji, Chih-Chung Wang, Ching-Yi Huang, Chia-Cheng Wu, Chia-Chun Lin and Chun-Yao Wang	National Tsing Hua University
2017	Low-Latency Voltage-Racing Winner-Take-All (VR-WTA) Circuit for Acceleration of Learning Engine	Chai-Heng Wu, Ting-Sheng Chen, Ding-Yuan Lee, Tsung-Te Liu, and An-Yeu (Andy) Wu	National Taiwan University, Taiwan
	Robust Test Pattern Generation for Hold-time Faults in Nanometer Technologies	Yu-Hao Ho, Yo-Wei Chen, Chih-Ming Chang, Kai-Chieh Yang, and Chien-Mo Li	National Taiwan University, Taiwan
2016	A 7 GB/S Half-Rate Clock and Data Recovery Circuit with Compact Control Loop	Yu-Po Cheng, Yen-Long Lee, Ming-Hung Chien, and Soon-Jyh Chang	National Cheng Kung University, Taiwan
	Overlay-aware Layout Legalization for Self-Aligned Double Patterning Lithography	Chong-Meng Huang and Shao-Yun Fang	National Taiwan University of Science and Technology, Taiwan
2015	A 127 fJ/conv. Continuous-Time Delta-Sigma Modulator with a DWA-Embedded Two-Step Time-Domain Quantizer	Chan-Hsiang Weng, Tzu-An Wei, and Tsung-Hsien Lin	National Taiwan University, Taiwan
	Clock-Domain-Aware Test for Improving Pattern Compression	Kun-Han Tsai and Janusz Rajski	Mentor Graphics, USA
2014	A 3.5-4GHz FMCW Radar Transceiver Design with Phase-Domain Oversampled Ranging by Utilizing a 1-bit Delta-Sigma TDC	Wei Zhang, Yizhi Han, Fei Chen,Bo Zhou, Xican Chen, Woogeun Rhee, and Zhihua Wang	Tsinghua University, China

	Thermal-aware Dynamic Buffer Allocation for Proactive routing Algorithm on 3D Network-on-Chip Systems	Yuan-Sheng Lee, Hsien-Kai Hsin, Kun-Chih Chen, En-Jui Chang, and An-Yeu Wu	National Taiwan University, Taiwan
2013	Worst-Case IR-Drop Monitoring with 1GHz Sampling Rate	Chen-Hsiang Hsu, Shi-Yu Huang, Ding-Ming Kwai, and Yung-Fa Chou,	National Tsing Hua University, Taiwan
2012	IMITATOR: A Deterministic Multicore Replay System with Refining Techniques	Shing-Yu Chen, Chi-Neng Wen, Geng-Hau Yang, Wen-Ben Jone, and Tien-Fu Chen	National Chiao Tung University, Taiwan
	A Monolithic 1.85GHz 2-stage SiGe Power Amplifier with Envelope Tracking for Improved Linear Power and Efficiency	Ruili Wu, Yan Li, Jerry Lopez, and Donald Y. C. Lie	Texas Tech. University, USA
2011	Important Test Selection For Screening Potential Customer Returns	Nik Sumikawa, Dragoljub Gagi Drmanac, LeRoy Winemberg, Li-C. Wang, and Magdy S. Abadir	University of California, Santa Barbara, USA
	A Macro-Layer Level Fully Parallel Layered LDPC Decoder SOC for IEEE 802.15.3c Application	Zhixiang Chen, Xiao Peng, Xiongxin Zhao, Qian Xie, Reona Okmura, Dajiang Zhou, and Satoshi GoTo	Waseda University, Japan
2010	Traffic-Thermal Mutual-Coupling Co-Simulation Platform for Three-Dimensional Network-on-Chip	Kai-Yuan Jheng, Chih-Hao Chao, Hao-Yu Wang, and An-Yeu Wu	National Taiwan University, Taiwan
2009	A 6-GS/s, 6-bit, at-speed testable ADC and DAC pair in 0.13μm CMOS	Chen-Kang Ho and Hao-Chiao Hong	National Chiao Tung University, Taiwan